WHAT IS CLAIMED IS:

1. A method for reprogramming a memory in a microcontroller, comprising the steps of:

providing a first memory, said first memory storing program instructions that the microcontroller is capable of executing;

providing a second memory, said second memory storing information;

identifying a pre-determined bit in a register, wherein a logical value of said pre-determined bit determines a first logical location of said first memory and a second logical location of said second memory;

altering said information of said second memory to produce altered information;

changing said logical value of said pre-determined bit in said register; and

responsive to said step of changing, interchanging said first logical location of said first memory with said second logical location of said second memory.

2. The method according to claim 1, wherein the reprogramming comprises:

in-system reprogramming.

3. The method according to claim 1, wherein said step of changing actuates a system reset.

4. The method according to claim 1, wherein said first and second memories comprise:

Random Access Memories.

5. The method according to claim 1, wherein said step of altering said information comprises the step of:

storing instructions to said second memory to produce said altered information.

6. The method according to claim 1, wherein said program instructions comprise:

vector instructions.

7. The method according to claim 1, further comprising the step of:

responsive to said step of interchanging, executing said altered information of said second memory from said first logical location.

8. The method according to claim 1, wherein said step of identifying a pre-determined bit comprises the step of:

identifying a battery-backed pre-determined bit.

9. The method according to claim 1, wherein said second memory comprises:

an external program memory.

10. The method according to claim 1, wherein said second memory comprises:

an internal program memory.

11. A method for interchanging the function of at least two memories, comprising the steps of:

assigning a first memory to a first logical location;

assigning a second memory to a second logical location;

utilizing said first memory for a first operation type;

utilizing said second memory for a second operation type;

adjusting a memory indicator; and

responsive to said step of adjusting, utilizing said first memory for said second operation type and said second memory for said first operation type.

12. The method according to claim 11, wherein said step of adjusting comprises the step of:

changing a bit in a register.

13. The method according to claim 11, wherein said first operation type comprises:

an instruction code access.

14. The method according to claim 11, wherein said second operation type comprises:

a data access.

15. The method according to claim 11, further comprising the step of:

responsive to said step of adjusting a memory indicator, actuating a system reset.

16. An arrangement for reprogramming a memory of a microcontroller, comprising:

a first memory, said first memory for storing program instructions to be executed by the microcontroller, wherein said first memory is assigned to a first logical location;

a second memory, said second memory for storing data information, wherein said second memory is assigned to a second logical location;

a pre-determined bit, said pre-determined bit for controlling assignment of said first and second logical locations to said first and second memories; and

a logical value associated with said pre-determined bit, said logical value determining logical location of said first memory, wherein changing of said logical value interchanges said first logical location of said first memory with said second logical location of said second memory.

17. The arrangement according to claim 16, wherein complementing said pre-determined bit resets the system.

18. The arrangement according to claim 16, wherein, responsive to interchanging said first logical location of said first memory with said second logical location of said second memory, said second memory stores program instructions to be executed by the microcontroller.

19. The arrangement according to claim 16, wherein said reprogramming comprises:

in-system programming.

20. The arrangement according to claim 16, wherein said first memory comprises:

a lowest 1K of internal program memory space.

21. The arrangement according to claim 16, wherein said pre-determined bit is located within a register.

22. The arrangement according to claim 16, wherein said pre-determined bit is battery backed.

23. The arrangement according to claim 16, wherein said first memory stores reset and interrupt vectors.

24. The arrangement according to claim 16, wherein said pre-determined bit requires Timed Access Operation.

25. A method for providing protected reprogramming of a memory in an electronic device, the method comprising the steps of:

providing a first memory, said first memory storing program instructions that the microcontroller is capable of executing;

providing a second memory, said second memory storing information;

identifying a pre-determined bit in a register, said pre-determined bit determining storage to said first memory and said second memory;

altering said information of said second memory to produce altered information;

changing a logical value of said pre-determined bit in said register; and

responsive to said step of changing, storing said altered information of said second memory in said first memory, thereby allowing for the protected reprogramming of said first memory.

26. An electronic device for providing a safeguard against unexpected loss of data during memory reprogramming, the electronic device comprising:

a first memory, said first memory for storing program instructions, wherein said first memory is assigned to a first logical location;

a second memory, said second memory for storing data information, wherein said second memory is assigned to a second logical location;

a pre-determined bit, said pre-determined bit for controlling assignment of said first and second logical locations to said first and second memories; and

a logical value associated with said pre-determined bit, wherein changing said logical value interchanges said first logical location of said first memory with said second logical location of said second memory.

27. A microcontroller for providing protected reprogramming of a memory, the microcontroller comprising:

a first memory, said first memory for storing program instructions, wherein said first memory is assigned to a first logical location;

a second memory, said second memory for storing data information, wherein said second memory is assigned to a second logical location;

a register, said register for storing memory bits associated with said first and second memories;

a memory select bit, said memory select bit stored in said register and having a logical value, said memory select bit further controlling assignment of said first and second logical locations to said first and second memories; and

wherein, changing said logical value associated with said memory select bit interchanges said first logical location of said first memory with said second logical location of said second memory.

28. An electronic device for reprogramming a memory, comprising:

means for providing a first memory and a second memory, said first memory storing program instructions, said second memory storing information;

means for identifying a pre-determined bit in a register, wherein a logical value of said pre-determined bit determines a first logical location of said first memory and a second logical location of said second memory;

means for altering said information of said second memory to produce altered information;

means for changing said logical value of said pre-determined bit in said register; and

means for interchanging said first logical location of said first memory with said second logical location of said second memory.

29. An arrangement for interchanging the functions of at least two memories within an electronic device, the electronic device comprising:

means for assigning a first memory to a first logical location;

means for assigning a second memory to a second logical location;

means for utilizing said first memory for a first operation type;

means for utilizing said second memory for a second operation type;

means for adjusting a memory indicator; and

means for utilizing, responsive to said step of adjusting, said first memory for said second operation type and said second memory for said first operation type.

30. The arrangement of claim 29, wherein said first and second memories comprise:

Flash memories.

31. The arrangement of claim 29, wherein said memory indicator comprises:

a nonvolatile memory cell.

32. The arrangement of claim 29, wherein said memory indicator can be reset by a Memory Management Unit.

33. The arrangement of claim 29, wherein said means for adjusting said memory indicator further comprises:

means for resetting said first and second memories.

34. An arrangement for altering a memory-addressing scheme of a memory, the arrangement comprising:

a first memory having a first memory location with address X;

a second memory having a second memory location with address Y; and

a pre-determined bit associated with said first memory and said second memory, said pre-determined bit having a logical value, wherein said logical value, when changed, assigns said first memory to said second memory location with address Y and said second memory to said first memory location with address X.

35. A method for manipulating the logical address locations of two memories in an electronic device, the method comprising the steps of:

assigning a first memory to a first set of logical address locations ranging from W to X;

assigning a second memory to a second set of logical address locations ranging from Y to Z;

designating a memory indicator to determine allocation of said first set of logical address locations and said second set of logical address locations to said first and second memories; and

adjusting said memory indicator such that said first set of logical address locations ranging from W to X are assigned to said second memory and said second set of logical address locations ranging from Y to Z are assigned to said first memory.

36. The method according to claim 35, wherein said first set of logical address locations ranging from W to X correspond to logical address locations ranging from 0 to M and said second set of logical address locations ranging from Y to Z correspond to logical address locations (M+1) to 2M.

37. The method according to claim 36, wherein said step of adjusting said memory indicator such that said first set of logical address locations ranging from W to X are assigned to said second memory and said second set of logical address locations ranging from Y to Z are assigned to said first memory further comprises the steps of:

adding M to any incoming address ranging from 0 to M; and

subtracting M from any incoming address ranging from (M+1) to 2M.

38. The method according to claim 35, wherein said step of adjusting said memory indicator such that said first set of logical address locations ranging from W to X are assigned to said second memory and said second set of logical address locations ranging from Y to Z are assigned to said first memory further comprises the steps of:

re-routing incoming memory access requests corresponding to said first set of logical address locations ranging from W to X to said second memory; and

re-routing incoming memory access requests corresponding to said second set of logical address locations ranging from Y to Z to said first memory.